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| 10/708,515 | 03/09/2004 | Ronald L. Gordon | FIS920030380 | 2514 |

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LAW OFFICE OF DELIO & PETERSON, LLC.
121 WHITNEY AVENUE
NEW HAVEN, CT 06510

| EXAMINER |
|---|
| RASHID, DAVID |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/708,515 | GORDON ET AL. | |
| | Examiner | Art Unit | |
| | David P. Rashid | 2624 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *16 January 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1,3-10,12-16 and 18-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3-10, 12-16, and 18-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12/14/2007* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

1. All of the examiner's suggestions presented herein below have been assumed for examination purposes, unless otherwise noted.

### *Continued Examination Under 37 CFR 1.114*

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on January 16, 2008 has been entered.

### *Amendments*

3. This office action is responsive to the claim amendment received on December 14, 2007. Claims 1, 3-10, 12-16, and 18-20 remain pending.

### *Drawings*

4. The replacement drawings were received on December 14, 2007 and are acceptable. In response to applicant's drawing amendments and remarks, the previous drawing objections are withdrawn.

### *Claim Rejections - 35 USC § 103*

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. **Claims 1, 3, 8- 10, 12, 16,** and **18** are rejected under 35 U.S.C. 103(a) as being unpatentable over Robles et al. (US 2004/0005089 A1) in view of Papadopoulou et al. (US 6,178,539 B1).

7. Regarding **claim 1**, while Robles discloses a method of creating a photomask layout (FIG. 5) for projecting an image of an integrated circuit design (paragraphs [0003], [0004]) comprising:

creating a layout (FIG. 3) of spaced (FIG. 3, element 315) integrated circuit shapes (FIG. 3, elements 310, 320) to be projected via the photomask;

creating bisectors ("centered between them" and "at some predetermined distances" in paragraph [0017] for the SRAF's to be placed) next to the spaced integrated circuit shapes;

determining bisectors ("centered between them" and "at some predetermined distances" in paragraph [0017]) between adjacent ones (FIG. 3) of the spaced integrated circuit shapes, the bisectors comprising locus of points equidistant from edges of the adjacent spaced integrated circuit shapes ("SRAF 335 centered between them", paragraph [0017] suggested that the bisector from which the SRAF has been placed is equidistant because it is "centered", as also supported in FIG. 3) and defining shared boundaries (the bisectors from which SRAF's are placed "define" shared boundaries, seeing an SRAF tells one of ordinary skill in the art that there is a shared boundary between the two edges); and

creating sub-resolution assist features (FIG. 3, elements 335, 355) along at least some of the bisectors between the adjacent ones of the spaced integrated circuit shapes, the sub-resolution assist features (FIG. 3, elements 335, 355) extending along the bisectors beyond (both SRAF elements 335 and 355 extend collectively beyond element 320) an adjacent spaced integrated circuit shape (FIG. 3, element 320), Robles does not teach

(i) creating Voronoi cells around the spaced integrated circuit shapes;

(ii) the bisectors defining shared boundaries of the adjacent Voronoi cells; and

(iii) extending a SRAF along a bisector beyond an adjacent spaced integrated circuit shape.

Papadopoulou discloses determining critical area for circuit layouts using Voronoi diagrams (FIG. 22) that teaches

creating a layout of spaced integrated circuit shapes (polygons in FIG. 5);

creating Voronoi cells (FIG. 5) around the spaced integrated circuit shapes;

determining bisectors (the bold lines of FIG. 5; FIG. 4 arrow) between adjacent ones of the spaced integrated circuit shapes, the bisectors comprising locus of points equidistant (Col. 5, line 66 – Col. 6, line 2) from edges of the adjacent spaced integrated circuit shapes and defining shared boundaries (defining the shared boundary is the bold bisector line/arrow itself in FIG. 4, FIG. 5, and so forth) of adjacent Voronoi cells,

wherein the bisectors between adjacent ones of the spaced integrated circuit shapes extend beyond an adjacent integrated circuit shape (FIG. 11, lowest horizontal bisector is longer in length than the immediate circuit shape above it).

It would have been obvious to one of ordinary skill in the art at the time the invention was made

(i) for the method of Robles to include creating Voronoi cells around the spaced integrated circuit shapes as taught by Papadopoulou;

(ii) for the bisectors at predetermined distances of Robles to be the bisectors determined from the Voronoi cells as taught by Papadopoulou; and

(iii) for the SRAFs of Robles to be placed on the Voronoi cell bisectors of Papadopoulou in such as way as to extend beyond an adjacent integrated circuit shape (as the Voronoi cells already extend beyond the integrated circuit shapes) as "[t]he present disclosure further describes a method for speeding up the grid method of Wagner and Koren, in the above referenced article. The method is based on a low polynomial algorithm to compute critical area for shorts accurately in irregular

rectilinear layouts.", Papadopoulou, Col. 5, lines 14 – 19 and that "[t]he method is presented for rectilinear layouts but it is extendible to general layouts.", Papadopoulou, Col. 5, lines 13 – 14 and "for computing critical area for shorts of a layout, in accordance with the present invention, includes the steps of computing a Voronoi diagram for the layout, computing a second order Voronoi diagram to arrive at a partitioning of the layout into regions, computing critical area within each region and summing the critical areas to arrive at a total critical area for shorts in the layout." , Papadopoulou, Col. 2, lines 58-64.

8. Regarding **claim 3**, Robles discloses wherein the adjacent ones of the spaced integrated circuit shapes (FIG. 3, elements 310, 320 wherein the elements are "adjacent") are parallel to each other (elements 310 and 320 are also parallel to each other) and the sub-resolution assist features (FIG. 3, elements 335, 355) along the bisectors ("centered between them" and "predetermined distances" in paragraph [0017]) are parallel (FIG. 3, element 335 is parallel to elements 310 and 335) to the spaced integrated circuit shapes.

9. Regarding **claim 8**, Robles discloses wherein the integrated circuit shapes (FIG. 3, elements 310, 320) are two-dimensional (elements 310, 320 in FIG. 3 are two-dimensional) and include shapes having edges parallel (FIG. 3, elements 330/350 and 340 are parallel) and perpendicular (elements 310 and 320 in FIG. 3 contain edges other than edges 330/350 and 340 that are perpendicular) to each other, between which the bisectors are located (FIG. 3, elements 335, 355).

10. Regarding **claim 9**, Robles discloses wherein the integrated circuit shapes (FIG. 3, elements 310, 320) are two-dimensional (elements 310, 320 in FIG. 3 are two-dimensional) and include shapes having lengths of parallel edges (FIG. 3, elements 330 and 340 are parallel) in which an edge of one shape ends at a point (the bottom point of edge 340 in FIG. 3) within the length of the other shape

(FIG. 3, element 330 continues to extend beyond the bottom point of edge 340 unto edge 350), between which the bisectors are located (FIG. 3, elements 335, 355).

11. Regarding **claim 10**, claim 1 recites identical features as in the program storage device readable by a machine, tangibly embodying a program of instructions executable by the machine to perform method steps (FIG. 11, FIG. 12) as in claim 1. Thus, references/arguments equivalent to those presented above for claim 1 are equally applicable to claim 10.

12. Regarding **claim 12**, claim 3 recites identical features as in claim 12. Thus, references/arguments equivalent to those presented above for claim 3 are equally applicable to claim 12.

13. Regarding **claim 16**, claim 1 recites identical features as in the article manufacture comprising a computer-usable medium having computer readable program codes means embodied therein (FIG. 11, FIG. 12) as in claim 1. Thus, references/arguments equivalent to those presented above for claim 1 are equally applicable to claim 10. All means-plus-function language is anticipated by Robles (FIG. 11, FIG. 12).

14. Regarding **claim 18**, claim 3 recites identical features as in claim 18. Thus, references/arguments equivalent to those presented above for claim 3 are equally applicable to claim 18.

15. **Claims 4, 13,** and **19** are rejected under 35 U.S.C. 103(a) as being unpatentable over the Robles et al. (US 2004/0005089 A1) in view of Papadopoulou et al. (US 6,178,539 B1) and LaCour (US 2002/0155357 A1).

Regarding **claim 4**, while Robles in view of Papadopoulou discloses the method of claim 1, Robles in view of Papadopoulou does not teach identifying different types of vertices for the bisectors

prior to creating the sub-resolution assist features, and prioritizing creation of the sub-resolution assist features in accordance with the type of vertex.

LaCour discloses a prioritization application of resolution enhancement techniques (FIG. 6) that teaches identifying different types of vertices ("bars overlap to form a "+" structure" in paragraph [0057]; FIG. 6, element 610; paragraphs [0047] through [0052] where the vertices are either the "generating edges" and "facing edges" that may either be orthogonal or angled) for the bisectors (the bisectors being the lines from which the scattering bars of LaCour are being placed) prior to creating the sub-resolution assist features (the LaCour vertex listing in Col. 8, paragraphs [0047] through [0052] and [0057] has been already been created before the LaCour algorithm is implemented), and prioritizing creation ("the ends of both scattering bars can be shortened to provide a "L" structure" in paragraph [0057]; FIG. 6, element 612; paragraphs [0053] through [0056]) of the sub-resolution assist features in accordance with the type of vertex.

It would have been obvious to one of ordinary skill in the art at the time the invention was made for the method of Robles in view of Papadopoulou to identify different types of vertices for the bisectors prior to creating the sub-resolution assist features, and prioritize creation of the sub-resolution assist features in accordance with the type of vertex as taught by LaCour "to improve lithography tools to improve the fidelity of the lithography process.", LaCour, paragraph [0022].

16. Regarding **claim 13**, claim 4 recites identical features as in claim 13. Thus, references/arguments equivalent to those presented above for claim 4 are equally applicable to claim 13.

17. Regarding **claim 19**, claim 4 recites identical features as in claim 19. Thus, references/arguments equivalent to those presented above for claim 4 are equally applicable to claim 19. All means-plus-function language is anticipated by Robles (FIG. 11, FIG. 12).

18. **Claims 5-6, 14-15,** and **20** are rejected under 35 U.S.C. 103(a) as being unpatentable over the Robles et al. (US 2004/0005089 A1) in view of Papadopoulou et al. (US 6,178,539 B1) and Lucas et al. (US 2004/0248016 A1).

19. Regarding **claims 5** and **6**, while Robles in view of Papadopoulou discloses the method of claim 1, Robles in view of Papadopoulou does not teach extending at least some of the sub-resolution assist features beyond the bisectors on which they are created to connect to other sub-resolution assist features.

Lucas discloses a method of designing a reticle and forming a semiconductor device therewith (paragraph [0006]) that extends (paragraph [0016]) at least some of the sub-resolution assist features (FIG. 3; element 56; FIG. 9, element 156) beyond the bisectors on which they are created to connect (FIG. 9, element 154) to other sub-resolution assist features (FIG. 3, element 52; FIG. 9, element 152).

It would have been obvious to one of ordinary skill in the art at the time the invention was made for the method of Robles in view of Papadopoulou to extend at least some of the sub-resolution assist features beyond the bisectors on which they are created to connect to other sub-resolution assist features as taught by Lucas "...for improved coverage of the assist features with improved process margin and reduced reticle inspection issues.", Lucas, paragraph [0023].

20. Regarding **claim 14**, claim 5 recites identical features as in claim 14. Thus, references/arguments equivalent to those presented above for claim 5 are equally applicable to claim 14.

21. Regarding **claim 15**, claim 6 recites identical features as in claim 15. Thus, references/arguments equivalent to those presented above for claim 6 are equally applicable to claim 15.

22. Regarding **claim 20**, claim 5 recites identical features as in claim 20. Thus, references/arguments equivalent to those presented above for claim 5 are equally applicable to claim 20.

23. **Claim 7** is rejected under 35 U.S.C. 103(a) as being unpatentable over the Robles et al. (US 2004/0005089 A1) in view of Papadopoulou et al. (US 6,178,539 B1) and Frankowsky (US 2002/0182523 A1).

24. Regarding **claim 7**, while Robles in view of Papadopoulou discloses the method of claim 1, Robles in view of Papadopoulou does not teach removing at least one of the sub-resolution assist features along the bisectors prior to finalizing the photomask layout.

Frankowsky discloses a method for carrying out a rule-based optical proximity correction with simultaneous scatter bar insertion (paragraph [0015]) that removes at least one of the sub-resolution assist features along the bisectors prior to finalizing the photomask layout (paragraph [0089]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made for the method of Robles in view of Papadopoulou to remove at least one of the sub-resolution assist features along the bisectors prior to finalizing the photomask layout as taught by Frankowsky because "[i]f these scatter bars were not removed, they would be imaged on the substrate in the exposure process in certain circumstances, which is undesirable.", Frankowsky, paragraph [0089].

***Response to Arguments***

25. Applicant's arguments filed on 9/14/2007 with respect to claims 1, 3-10, 12-16, and 18-20 have been respectfully and fully considered, they are not found persuasive.

26. Summary of Remarks regarding claims 1-3, 8-10, 12, and 16-18:

Applicant argues Robles simply makes no mention of any bisector or SRAF that extends beyond its features 310 or 320. Robles in fact teaches away from applicants' invention since the

SRAFs 355 that do extend beyond feature 320 are at distances other than the bisector between features 310 and 320.

The Papadopoulou patent does not remedy the deficiencies of Robles. The Papadopoulou patent does mention the use of Voronoi diagrams, but uses the diagrams to compute critical areas for shorts between different conducting regions of a layout. Papadopoulou does not use any boundaries of Voronoi cells to create sub-resolution assist features, as in applicants' claimed invention. Accordingly, one of ordinary skill in the art would not even look to combine the Robles and Papadopoulou references in the first instance.

Even if the references were combined, there is no suggestion in either Robles or Papadopoulou to create a bisector that comprises the locus of points equidistant from edges of the adjacent spaced integrated circuit shapes and defines shared boundaries of adjacent Voronoi cells, or to create a SRAF that extends along the bisectors beyond an adjacent spaced integrated circuit shape. Robles does not disclose or suggest a bisector or SRAF that extends beyond the end of a feature edge, as applicants claim. Papadopoulou does not disclose or suggest creating bisectors or SRAFs along shared boundaries of adjacent Voronoi cells. As such, one skilled in this art would not arrive at applicants' claimed invention from the hypothetical combination of these references. Applicants submit that claims 1, 10 and 16 are therefor not obvious from Robles in view of Papadopoulou. (Applicant Resp. 10, December 14, 2007.)

27. Examiner's Response regarding claims 1-3, 8-10, 12, and 16-18:

Suggestion

The Examiner suggests that adding in the limitation that each SRAF must have a length at least five times its width, and those that violate this rule are deleted to the independent claims may overcome all the current prior art of record.

Argument I

However, Robles makes no mention of every bisector or SRAF that cannot extend beyond its features which enables an operable combination when using the bisectors from the Voronoi cells of Papadopoulou (which do in fact extend beyond its features). Papadopoulou does in fact remedy the deficiencies of Robles. On much broader reasoning, the Examiner asserts that it would have been obvious to develop another bisector algorithm (such as using Voronoi cells as taught by Papadopoulou) within the objective of Robles for creating a photomask. SRAFs need a bisector algorithm to be placed unto the photomask, and it would have been obvious to use the Voronoi cells of Papadopoulou to do so. In specific, FIG. 11 of Papadopoulou shows such a bisector between two integrated circuit shapes that extends beyond the integrated circuit shapes. It would have been obvious to one of ordinary skill in the art at the time the invention was made for place an SRAF on top of this bisector, which would ultimately be an SRAF that extends beyond an adjacent spaced integrated circuit shape. This combination is entirely operable in view of the broadness of the claims in question.

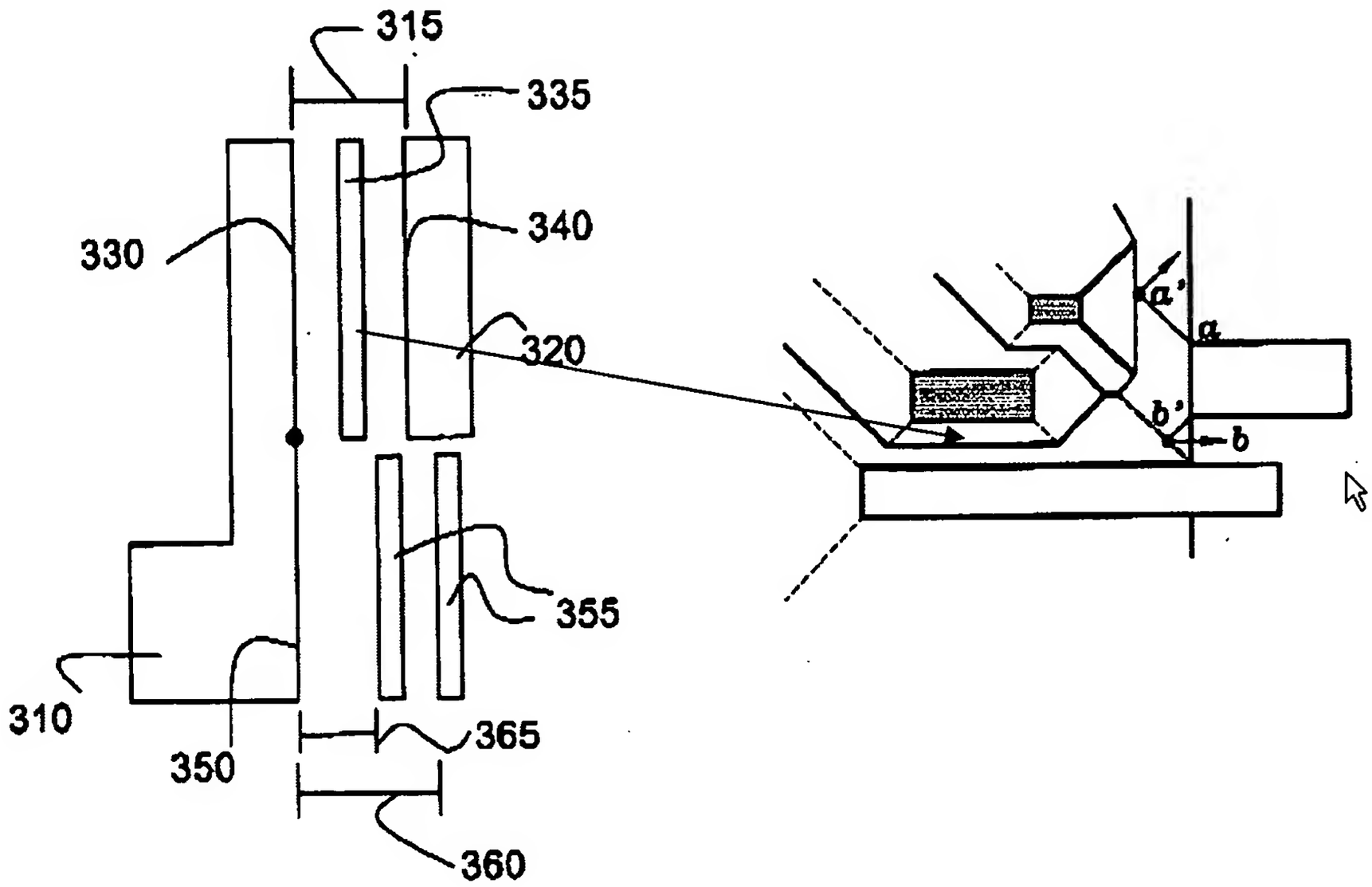


FIG. 11

It would have been obvious to one of ordinary skill in the art at the time the invention was made

(i) for the method of Robles to include creating Voronoi cells around the spaced integrated circuit shapes as taught by Papadopoulou;

(ii) for the bisectors at predetermined distances of Robles to be the bisectors determined from the Voronoi cells as taught by Papadopoulou; and

(iii) for the SRAFs of Robles to be placed on the Voronoi cell bisectors of Papadopoulou in such as way as to extend beyond an adjacent integrated circuit shape (as the Voronoi cells already extend beyond the integrated circuit shapes) as "[t]he present disclosure further describes a method for speeding up the grid method of Wagner and Koren, in the above referenced article. The method is based on a low polynomial algorithm to compute critical area for shorts accurately in irregular rectilinear layouts.", Papadopoulou, Col. 5, lines 14 – 19 and that "[t]he method is presented for rectilinear layouts but it is extendible to general layouts.", Papadopoulou, Col. 5, lines 13 – 14 and

"for computing critical area for shorts of a layout, in accordance with the present invention, includes the steps of computing a Voronoi diagram for the layout, computing a second order Voronoi diagram to arrive at a partitioning of the layout into regions, computing critical area within each region and summing the critical areas to arrive at a total critical area for shorts in the layout." , Papadopoulou, Col. 2, lines 58-64.

Argument II

Claim 1, lines 11-13 cite the newly added limitation: "the sub-resolution assist features extending along the bisectors beyond an adjacent spaced integrated circuit shape" (*emphasis added*). The claim can also be interpreted as allowing a combination of SRAFS that as a whole would extend along the bisectors beyond an adjacent spaced integrated circuit shape (and not just one SRAF as the Applicant is trying to interpret and limit). Both SRAFs 335 and 355 of Robles extend beyond integrated circuit shape 320 in FIG. 3 in combination and are "adjacent to it", thus SRAFs extend along the bisectors beyond an adjacent spaced integrated circuit shape. The rejection holds in view of this interpretation also.

28. Summary of Remarks regarding claims 4, 13 and 19:

Applicant argues LaCour mentions no "vertex" of a bisector, let alone a "bisector" as applicants' have defined. While LaCour does describe classifying scattering bars into priority groups, such classification has nothing to do with the type of vertices of bisectors, as applicants have defined. Therefore, claims 4, 13 and 19 would not be obvious to one of ordinary skill in the art. (Resp. 11.)

29. Examiner's Response regarding claims 4, 13 and 19:

However, "vertex" is defined as "a point…that...comprises the intersection of two or more lines...". *See* Merrian-Webster Online, 2007-2008, "vertex" n. def. 2b, *available at* http://www.m-w.com/dictionary. "Bisector" is defined as "one that bisects; *especially*: a straight line that bisects an

angle or a line segment". *See* Merrian-Webster Online, 2007-2008, "bisect" n. LaCour clearly discloses vertexes and bisectors in view of the respective definitions and does not require the actual words "vertex" and "bisector".

Robles in view of Papadopoulou uses the Voronoi algorithm to create "vertices for the bisectors" (all vertices as shown in FIG. 5 or FIG. 11, Papadopoulou). LaCour does in fact describe classification with the type of vertices of bisectors (e.g. a "+" shaped vertex is changed to "L" shaped as described in the rejection above). It would have been obvious to one of ordinary skill in the art at the time the invention was made for the method of Robles in view of Papadopoulou to identify different types of vertices for the bisectors prior to creating the sub-resolution assist features, and prioritize creation of the sub-resolution assist features in accordance with the type of vertex as taught by LaCour "to improve lithography tools to improve the fidelity of the lithography process.", LaCour, paragraph [0022].

30. Summary of Remarks regarding claims 5, 6, 14, 15, and 20:

Applicant argues Lucas makes no mention of extending sub-resolution assist features beyond bisectors as defined by applicants. Lucas does not disclose or suggest the extension of sub-resolution assist features along bisectors defined by shared boundaries of adjacent Voronoi cells. Lucas merely links sub-resolution assist features in a manner unrelated to applicants' claimed method. Accordingly, there is no disclosure of applicants' claimed method in the combination of Robles and Lucas. (Resp. 11-12.)

31. Examiner's Response regarding claims 5, 6, 14, 15, and 20:

A Varanoi bisector of Robles in view of Papadopoulou would eventually stop before coming into "contact" with a circuit feature edge, as supported in FIG. 3, element 56 of Lucas. FIG. 9, element 162 of Lucas extends the SRAF outside the limitations of the Varanoi bisector of Robles in

view of Papadopoulou. It would have been obvious to one of ordinary skill in the art at the time the invention was made for the method of Robles in view of Papadopoulou to extend at least some of the sub-resolution assist features beyond the bisectors on which they are created to connect to other sub-resolution assist features as taught by Lucas "...for improved coverage of the assist features with improved process margin and reduced reticle inspection issues.", Lucas, paragraph [0023].

32. Summary of Remarks regarding claim 7:

Applicant argues dependent claim 7 recites removing at least one of the sub-resolution assist features along the bisectors prior to finalizing the photomask layout. Frankowsky does not disclose or suggest the removal of sub-resolution assist features along bisectors defined by shared boundaries of adjacent Voronoi cells. Frankowsky merely removes scatter bars in a manner unrelated to applicants' claimed method. Therefore, there is no disclosure of applicants' claimed method in the combination of Robles and Frankowsky. (Resp. 12.)

33. Examiner's Response regarding claim 7:

Just because Frankowsky removes scatter bars in a manner unrelated to applicants' claimed method does not prohibit its anticipation to the claim in question that requires "removing at least one of the sub-resolution assist features along the bisectors prior to finalizing the photomask layout".

Frankowsky gives a clear motivation of why it would have been obvious to one of ordinary skill in the art at the time the invention was made for the method of Robles in view of Papadopoulou to remove at least one of the sub-resolution assist features along the bisectors prior to finalizing the photomask layout as taught by Frankowsky because "[i]f these scatter bars were not removed, they would be imaged on the substrate in the exposure process in certain circumstances, which is undesirable.", Frankowsky, paragraph [0089].

***Conclusion***

34. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US 5491641 A; US 5821014 A; US 5880970 A; US 6317859 B1; US 6335130 B1; US 20020001758 A1; US 6413683 B1; US 20020155357 A1; US 6503666 B1; US 6541167 B2.

35. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David P. Rashid whose telephone number is (571) 270-1578. The examiner can normally be reached Monday - Friday 8:30 - 17:00 ET.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vikkram Bali can be reached on (571) 272-7415. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/David P. Rashid/
Examiner, Art Unit 2624

VIKKRAM BALI
PRIMARY EXAMINER

David P Rashid
Examiner
Art Unit 2624